

ATLAS Technical Coordination
Radiation Hardness Assurance
Reporter: M. Dentan.

Report of the
First meeting of the ATLAS Radiation Hardness Assurance Working Group
CERN, 40-R-C10, 3 September 1999, 9:00-17:00.

Agenda:

1. Introduction. Speaker: Martin Dentan
 - Goal of the RHA-WG;
 - Organization.
2. Radiation Hardness Assurance made by ATLAS sub-detectors collaborations:
 - Muon Collaboration. Speaker: Robert Richter;
 - Tile Collaboration. Speaker: Philippe Rosnet;
 - LAR Collaboration. Speaker: Christophe De la Taille;
 - TRT Collaboration;
 - SCT Collaboration. Speaker: Jan Kaplon;
 - Pixel Collaboration. Speaker: Attilio Andreazza.
3. Total dose and displacement effects.
Invited speaker: Olivier Musseau (CEA-DAM);
4. SEE studies on GLINK candidates for the ATLAS LARG Calorimeter.
Speaker: Marie-Laure Andrieux;
5. SEE measurement on Pixel CMS DMILL chips.
6. Single event effects.
Invited speaker: Olivier Flament (CEA-DAM);
7. Discussion and decision:
 - Radiation levels, test procedures, COTS, voltage regulators;
 - Improvement and spreading of the knowledge on radiation effects within ATLAS;
 - Members of the RHA-WG within ATLAS subdetectors collaborations;
 - Open questions;
 - Decisions.

Attendees:

Attilio Andreazza (Bonn/Pixel), Marie-Laure Andrieux (Grenoble/LARG), Francis Anghinolfi (CERN/SCT), Robert Chadelas (Clermont/Tile), Christophe Delataille (Orsay/LARG), Martin Dentan (CERN/ATLAS TC), Federico Faccio (CERN/COTS), Philippe Farthouat (CERN/ATLAS TC), Olivier Flament (Invited expert/CEA-DAM), Jan Kaplon (CERN/SCT), Nachman Lupu (Haifa/Muons), Olivier Musseau (Invited expert/CEA-DAM), Robert Richter (Munich/Muons), Philippe Rosnet (Clermont/Tile), Giorgio Stefanini (CERN/CMS).

I. Introduction:

The radiation hardness of ATLAS electronics systems is a very challenging problem. Radiation produces various damages or destruction, which can be evaluated only by specific tests made by sampling on homogeneous batches of components. Without a precise analysis of the radiation hardness, some weaknesses to radiation – which may be very serious - could remain hidden until they appear on the electronics systems during their operation in ATLAS. Moreover, during its first years of operation, LHC will use a low luminosity beam, and the first problems due to radiation will probably not be seen before starting the high luminosity beam, probably in 2007 – about 8 years from today. At that time, the engineers in the collaborations responsible for the developments of ATLAS sub-detectors will be scattered; some of the chips will be obsolete; and it will be very difficult to correct or to rebuild any sub-systems. The only way to avoid such critical situations is to develop and to build all the ATLAS electronics systems with the aim of their high reliability versus irradiation effects. All the necessary and sufficient tests required to make sure that all the electronics systems will resist to the various radiation constraints must be done before starting the fabrication of those systems.

The aim of the ATLAS Radiation Hardness Assurance is to provide ATLAS sub-detector Collaborations with the rules and the help required to get this reliability of the electronics systems versus irradiation. Some of these rules already exist, provided by ATLAS Technical Co-ordination; some of them are yet to be established.

Goals and scope of the RHA Working Group:

- Help ATLAS sub-detectors Collaborations to define and apply a *common* strategy for the radiation hardness assurance;
- Minimize the work and maximize the reliability by using experience from the LHC experiments and other communities (space, defense, nuclear industry), by choosing solutions dedicated to LHC needs, and by sharing results between ATLAS subdetectors wherever possible.
- The first scope of the RHA-WG concerns electronics components (active and passive) and semiconductor sensors. In a second step, this scope could be extended to other sensors and mechanical components (cables, etc.).

Organization:

- The RHA-WG is constituted by the persons responsible for the radiation hardness assurance within each ATLAS sub-detectors collaborations, plus the ATLAS FEE Coordinators (P. Farthouat, B. Williams) and the RHA-WG Convener (M. Dentan). During the first meeting, ATLAS sub-detectors collaborations were represented by the attendees listed in the front page. A more formal nomination of the representatives of the ATLAS collaborations in the RHA-WG will be done later.
- The RHA-WG will work in collaboration with other groups or projects (COTS, RD49, LHC Experiments, ROSE), and with the other scientific communities involved in the domain of electronics radiation hardness (space, nuclear, ...).

II. Radiation Hardness Assurance made by the Sub-detector Collaborations:

1. Muon Collaboration. Speaker: R. Richter

The results presented during this meeting concern the power supply only. A global presentation of the radiation hardness assurance strategy of the Muon Collaboration is expected in the next RHA-WG meeting.

1.1. Summary of the studies made on power supplies:

Power supplies and other service equipment for the ATLAS sub-detectors can be located on the galleries in the UX hall, close to the FE electronics, instead of being in the USA15, which is about 80 m further away. This would lead to significant savings w.r.t. cost, power dissipation and space requirements, provided a sufficient amount of radiation tolerance of the respective electronics can be demonstrated.

As power supplies are the most cost-relevant part of electrical services, they have been studied first and some results are already available. As a general strategy, we did not attempt to qualify each component of a power supply individually w.r.t. rad-tolerance but rather tried to look at a given power supply as a unit. The idea was to identify faulty components after the potential failure of the unit, understand the damage mechanism and look for an improvement. In this spirit 14 commercial power supplies from 7 different vendors had been tested about 1 year ago at the Prospero facility (see below). The result was that most units failed between 10^{11} and 10^{12} n/cm². Post mortem analysis showed that all identified failures were due to optocouplers, which were used in the circuits. Replacing the optocoupler in a faulty unit by a new device brought it back to pre-rad. performance (operation fully inside specs).

Another important result, obtained in the meantime, was that HP optocouplers (HP6N138/139) proved to be about 10 times more rad-tolerant than the ones used in these tests and were functionally compatible with those.

To certify this result, a second test is now prepared where commercial power supplies are tested with optocouplers replaced by the HP device. The prediction is that all units will withstand at least $5 \cdot 10^{12}$ n/cm². As all relevant parameters are tested online during the irradiation, this can be verified immediately after the test. The date foreseen for this test is October 20th.

It should, however, be noted that, even with a positive outcome of this test, power supplies can not yet be considered fully qualified for reliable 10 year operation in the UX hall. The reason is that the energy spectrum of these fission neutrons goes hardly up to 3 MeV. It has been demonstrated (see presentation of M-L. Andrieux, chapter V, below) that higher energetic neutrons (e.g. in the 20 MeV range) can create regions of high local ionization in Silicon, about a factor of 10 more than typical fission neutrons are able to do. The consequences of high local ionization depends on the function of the device. Memories may show non-destructive SEU, while e.g. power MOSFETs may be

destroyed due to various failure modes (SEB, SEGR, see chapter VI, below). An irradiation test at a high energy n-source will therefore be mandatory and a run at the CERI facility is foreseen for early 2000.

1.2. Radiation levels:

Targeted doses and fluences are based on the ATLAS Technical Coordination Technical Design Report (ATLAS-TC-TDR), chapter 20.2, pp. 366-370. This document is based on radiation maps simulated by Mike Shupe.

The radiation environment at the outer circumference of the MDT chambers corresponds to about $2 \cdot 10^{11}$ n/cm² (1 MeV equiv.) and below a krad of ionizing radiation in 10 years of LHC operation. A safety factor of 4 is already included in these numbers.

1.3. Radiation facilities:

- Neutrons ($E_n < 3$ MeV; $\langle E_n \rangle = 0.75$ MeV) from ²³⁵U fission reactor (Prospero);
- Neutrons ($E_n < 40$ MeV) produced by a deuteron or a proton beam shooting a Be target (CERI).

1.4. Test Procedures:

- Radiation hardness tests procedures specially developed by Muon Collaboration.
- AC+DC measurements based on actual operating conditions;
- Measurements made on board;
- Measurements made during irradiation (on line) and after irradiation (off line).
- Tests dedicated to measure cumulated radiation effects (displacement damages).
- These tests do not cover SEE.

1.5. Test results:

- The failure of commercial power supplies irradiated with fission neutrons was in all cases traced back to faulty optocouplers, manufactured by Siemens or Toshiba.
- Tests on other optocouplers showed that HP 6N138/139 and HP CL-0731 (SMD package) gave far superior robustness to neutrons.

1.6. Future work:

- New neutron tests of the full power supplies equipped with HPCL-0731 optocouplers;
- SEE neutron tests of the full power supplies equipped with HPCL-0731 optocouplers;
- Full radiation hardness qualification (TID, NIEL, SEE) of the DCS (Detector Control System), of the LMB (Local Monitoring Box), of the CANbus, and of the front end boards of the Muon detectors (MDT, CSC, RPC and TGC).

2. Tile Collaboration. Speaker: Philippe Rosnet

2.1. List of components:

- The main functions contained in the Tile electronics boards are listed in appendix 1.

2.2. Radiation levels:

- a. Targeted doses and fluences used by Tile Collaboration for radiation tests are based on the ATLAS policy on radiation-tolerant electronics, including safety factors on simulations and on dose and fluence rate. This ATLAS policy is based on radiation maps simulated by Mike Shupe.
- b. Improved radiation simulations are required to take into account the material of the drawers containing the electronics boards.
- c. Question from Tile Collaboration: is it possible to reduce the effective radiation levels in the drawers by putting a polyethylene block in the fingers? What would be the resulting radiation level?

Items b. and c. require additional simulations and have been submitted to Mike Shupe.

2.3 Irradiation facilities:

- Photons from ^{60}Co source ();
- Neutrons ($E_n < 3 \text{ MeV}$; $\langle E_n \rangle = 0.75 \text{ MeV}$) from ^{235}U fission reactor (Prospero).
- Neutron source at Clermont (used for first tests, but no longer used).

2.4. Test procedures:

- Radiation hardness tests procedures specially developed by Tile Collaboration.
- AC+DC measurements based on actual operating conditions;
- Measurements made on board;
- Measurements made during irradiation (on line) and after irradiation (off line).
- Tests dedicated to measure cumulated radiation effects (ionization and displacement damages).
- These tests do not fully cover SEE (i.e. Single Event Effects, whose measurement require protons or pions beam).

2.5. Test results:

- See summary of the results in appendix 1 and with more details in the transparencies presented by P. Rosnet.
- Some components give good results, others need additional tests or are still to be tested.
- Full SEE tests are still to be done with protons or pions.

2.6. Future work:

- New neutron irradiation to test new possible solutions for the opto-couplers (end of September 99 at Prospero);
- Full photon (^{60}Co) and neutron irradiation tests on the Mother boards and on the digitizers were scheduled in summer 99 (no results available today, see next Tile Cal electronics meeting on September 10).

3/ **LAR Collaboration. Speaker: C. Delataille**

3.1. List of components:

- The main functions contained in the LAR electronics boards are listed in appendix 2.

3.2. Radiation levels:

- Targeted doses and fluences used by LAR Collaboration for radiation tests are based on the ATLAS policy on radiation-tolerant electronics, including safety factors on simulations and on dose and fluence rate. This ATLAS policy is based on radiation maps simulated by Mike Shupe.

3.3. Irradiation facilities:

- γ photons from ^{60}Co (Saclay);
- γ photons from ^{60}Co (BNL);
- Neutrons ($E_n < 40$ MeV) produced by a deuteron or a proton beam shooting a Be target (CERI).
- α particles (source to be defined).

3.4. Test procedures:

- Radiation hardness tests procedures specially developed by LAR Collaboration.
- AC+DC measurements based on actual operating conditions;
- Measurements made on board or on elementary device;
- Measurements made during irradiation (on line or periodical monitoring).
- Tests mostly dedicated to measure cumulated radiation effects (ionization and displacement damages).
- Some of these tests are also dedicated to measure SEE (bit error rate and upset tests using neutrons producing nuclear reaction in silicon, or using protons; latch-up tests using α particles).

3.5. Results:

- See summary of the results in appendix 2 and with more details in the transparencies presented by C. Delataille.

- Bit Error Rate (BER) measurements have been done on Glinks using neutron beams producing nuclear reaction in silicon. Preliminary results are satisfactory.
- SEE tests (BER, upsets, latch-up) will be done using proton or pion beams.
- Modified VICOR power supplies (equipped with transformers) are robust against TID and NIEL effects. SEGR (Single Event Effect Gate Rupture) tests must be done. These power supplies will be followed by rad-hard voltage regulators developed by ST for RD49 collaboration (CERN).

3.6. Future work:

- Migrations from COTS and FPGAs into DMILL;
- Ambitious milestone: first rad-hard ATLAS boards in 2001.

3.7. Summary of LAR Radiation Hardness Assurance proposed strategy:

- Critical ASICs are developed in DMILL to avoid any radiation hardness risk;
- FPGA should be migrated into DMILL;
- COTS are used only if there is absolutely no doubt on the radiation tolerance; in other cases, COTS are migrated into DMILL.

4/ TRT Collaboration:

- A presentation of the TRT radiation hardness assurance strategy is expected in the next RHA-WG meeting.

5/ SCT Collaboration. Speaker: Jan Kaplon

The results presented during this meeting concern the ABCD chip only. A global presentation of the SCT radiation hardness assurance strategy is expected in the next RHA-WG meeting.

5.1. List of components:

- The full list of components was not discussed during this meeting.
- Two solutions are developed to produce SCT ASICs:

Two chips solution:

- CAFE: Bipolar FE (amplifier + comparator) implemented in MAXIM technology;
- ABC: CMOS readout chip with binary pipeline, implemented in Honeywell (RICMOS IV process).

One chip solution:

- ABCD2T chip integrating bipolar FE and CMOS readout chip, implemented in DMILL.

5.2. Radiation levels:

- Targeted doses and fluences used by SCT Collaboration are based on radiation maps simulated by Mike Shupe.
- Total fluence of particles producing displacement damages: $1.5E14 \text{ cm}^{-2}$ (1 MeV equivalent neutron fluence) in 10 years of operation;
- Total dose deposited by ionizing particles: 10 Mrads in 10 years of operation.

5.3. Irradiation facilities:

- X-ray, 10 keV (CERN). 4-10 krad/mn;
- Protons, 24 GeV (PS-T7, CERN);
- Neutrons, 1 MeV (reactor, Ljubljana).

5.4. Test procedures:

- Radiation hardness tests procedures specially developed by SCT Collaboration.
- AC+DC measurements based on actual operating conditions;
- Measurements made on board or on elementary device;
- Measurements made during irradiation (on line monitoring in the case of R-ray tests) or after irradiation (off line monitoring in the case of proton tests).
- Tests mostly dedicated to measure cumulated radiation effects (ionization and displacement damages).
- Proton tests also give results on SEE sensitivity (but with one incident angle only).

5.5. Results:

ABCD2 (prototype of ABCD2T):

- After 10 Mrads, 12% speed degradation.

ABCD2T:

- After 10 Mrads, DAC Linearity better than +/- 0.7% and Amplifier + shaper ENC < 700 electrons (chip on pcb without detector).
- After $3E14 \text{ p/cm}^2$ (24 GeV), average gain 62 mV/fC and average noise 6 mv rms (hybridized chip). Also after $3E14 \text{ p/cm}^2$ (24 GeV), matching spread multiplied by three. This matching spread is fully corrected by using 4 bit trim-DAC implemented in each channel of the ABCD2T (matching meets the TDR specifications).

5.6. Future work:

- X-ray tests on ABCD2T from new batch to improve statistics;
- Proton irradiation on full SCT module at CERN.
- Neutron irradiation on full SCT module at Ljubljana and cross-checking with CERN proton tests.

6/ Pixel Collaboration. Speaker: A. Andreazza

The transparencies presented by Attilio Andreazza are available on the following web site: <http://home.cern.ch/~aandreaz/irradiation>

6.1. List of components:

- The main functions contained in the Pixel modules are listed in appendix 3.

6.2. Radiation levels:

- Targeted doses and fluences used by Pixel Collaboration are based on radiation maps simulated by Mike Shupe;
- Total fluence of particles producing displacement damages (NIEL): $6E14 \text{ cm}^{-2}$ (1 MeV equivalent neutron fluence) in 10 years of operation.
- Total dose deposited by ionizing particles: 30 Mrads in 10 years of operation.

6.3. Irradiation facilities:

- Protons, 24 Gev (PS-T7, CERN);
- Protons with lower energy (LBL).

6.4. Test procedures:

- Radiation hardness tests procedures specially developed by Pixel Collaboration.
- AC+DC measurements based on actual operating conditions;
- Measurements made on Pixel modules (hybrid) and on elementary ASIC or COTS;
- Measurements made during irradiation (when possible) or after irradiation.
- Tests dedicated to measure cumulated radiation effects (ionization and displacement damages).
- Tests mostly dedicated to measure cumulated radiation effects (ionization and displacement damages).
- Proton tests also give results on SEE sensitivity (but with one incident angle only).

6.5. Results:

- Most of the ASIC results will be obtained from DMILL batch expected in fall 99 (See appendix 3).

6.6. Summary of the Pixel Radiation Hardness Assurance proposed strategy:

- Use standard components which are intrinsically enough radiation tolerant (as for optical fibers and opto-packages);
- Develop ASICs in radiation-hard technologies: the design in DMILL for all the components is almost completed; Honeywell SOI processes is foreseen where additional integration is needed (B-layer).
- Develop dedicated designs and improved radiation-hard materials for the sensors (ATLAS pixel sensor group and ROSE Collaboration).

III. Total Dose and Displacement Damages Effects. Invited speaker: O. Flament

Olivier Flament, from CEA-DAM (Bruyeres-le-Chatel, France), is a specialist of TID and NIEL effects. He presented a summary of the mechanisms of degradation induced by irradiation in semiconductor materials and in elementary transistors, and their consequences in integrated circuits (see transparencies). Then he focused his talk on irradiation tests.

Ionizing irradiation tests:

The most critical parameters are:

- Total dose;
- Time after irradiation;
- Dose rate;
- Energy of the incident particles;
- Temperature;
- Biasing conditions.

Standard tests have been developed to evaluate the robustness of electronics against ionizing dose (DOD standard MIL883STD-1019.4 in the US; ESA standard 22900 in the EU). These tests can be done at elementary component level (transistor, ASIC) or at electronics board level. Based on a conservative approach (in certain cases, “good” parts could be rejected), they enable a reliable selection of radiation-hard parts. They can be used for both rad-hard or non rad-hard (“COTS”) devices.

Low dose rate increase irradiation effects. Theoretical models well correlated to experimental results enable to simulate low dose rate by post irradiation annealing, *on CMOS devices only*. Standard test procedures do exist to simulate low dose rate on CMOS devices. Unfortunately, good theoretical models for low dose rate do not exist for bipolar transistors, and the simulation of low dose rate by post irradiation annealing is generally not reliable for these devices.

Displacement damage tests:

These tests are generally performed using neutrons (which do not produce parasitic ionization).

In the LHC radiation environment, neutron irradiation effects will *not* depend on fluence rate (there is not “low fluence rate” effect) nor on time (there is not significant annealing after irradiation). The most critical parameters in neutron irradiation tests are:

- Total fluence (1 MeV equivalent neutron);
- Energy of the neutrons;
- Temperature.

Standard test procedures have been developed to evaluate the robustness of electronics against displacement damages (DOD standard MIL883STD-1017 in the US).

For both ionizing radiation effects and displacement damage effects, a predictive analysis of the radiation hardness at system level can be obtained by coupling standard irradiation tests to statistical analysis methods.

IV. SEE studies on GLINK candidates for the ATLAS LAR Calorimeter.

Speaker: Marie-Laure Andrieux

First model and radiation test:

System submitted to irradiation: optical link emitter

- Input data: 32 bit, 40 MHz;
- MUX => 16 bit, 80 MHz;
- G-link Tx (HDMP-1022);
- Driver + Laser (VCSEL);
- 50/125 GRIN optical fiber.

Constraint:

- Neutrons (SEE effects on components);
- Photons (no effects seen on components).

Mechanism of error generation (first model):

- Incident particle: neutrons (energy E_n);
- “n,p” reaction in silicon: a neutron shooting a silicon atom produces p + Al;
- “n, α ” reaction in silicon: a neutron shooting a silicon atom produces α + Mg;
- p and α induce instantaneous charge deposition in the silicon material from the optical link emitter;
- Instantaneous charge deposition produces upsets responsible for soft errors.

Irradiation test facility:

- CERI, Orleans, Fr: a deuteron beam shooting a Be target produces neutrons with a known spectrum and flux.

BER prediction:

- See details in appendix 4 and in transparencies presented by M.L. Andrieux.
- *Preliminary* results based on the first model: $BER_{(ATLAS)} = 1$ error every 30 min.

Second model (refined version of model 1) and radiation test :

- Same system and constraints, same irradiation test facility.
- The second model is based on the BGR (Burst Generation Rate) method. This method takes into account the microscopic cross section of neutrons (energy E_n) to produce recoil atoms (Energy E_r or greater) via different nuclear reactions. One of these nuclear reactions was studied in details in the first model.
- A more complete analysis of this model in the case of ATLAS optical links emitter is required to obtain reliable BER predictions.

V. SEE measurement on Pixel CMS DMILL chips

R. Horisberger apologize for not participating to this meeting. His talk will be presented at the next LEB meeting.

VI. Single Event Effects. Speaker: O. Musseau

Olivier Musseau, from CEA-DAM (Bruyeres-le-Chatel, France), is a specialist of Single Event Effects. He presented a detailed summary of the mechanisms of Single Event Effect induced by irradiation in semiconductor materials and in elementary transistors, and some of their consequences at system level (see transparencies).

The critical parameter governing SEE mechanisms are:

- LET (Linear Energy Transfer), or dE/dX , which depends on the incident particle and on its energy and on the semiconductor material;
- SEE cross section, which depends on the SEE mechanism, on the LET, on the incident angle of the particle producing SEE, on the bias voltage, on the layout (dimensions of the sensitive node), on the technology used (gate oxide thickness and minimum width and length), on the substrate (bulk material, bulk epitaxial material, SOI material).

When the track cross a reverse-biased junction, the charge deposition is strongly enhanced by the mechanism of “funneling”.

The main SEE are:

- Upset in a memory cell or in a logic circuit (non destructive effect);
- Latch-up (potentially destructive effect);
- SEB (Single event burnout, destructive effect);
- SEGR (Single Event Gate Rupture, destructive effect).

SEU can produce serious dysfunction at system level. Single Error SEU can be detected and corrected. Multiple Error SEE can cannot be corrected by usual parity controls. Such errors can be produced by a single particle entering the silicon surface with a fringing angle (its track can cross numerous sensitive nodes); or when the charge deposited by a particle entering the silicon surface with a normal angle hit several sensitive nodes (the occurrence of such multiple hit increases in advanced technologies because the minimum gate length decreases).

SEU sensitivity increases when the minimum gate length decreases (this is the case in advanced processes). This increasing sensitivity is mainly due to the decreasing bias voltage and the decreasing capacitance of the sensitive nodes. It can be partially limited by increasing the capacitance of the sensitive nodes, using a special layout (this solution is detrimental to the integration density).

Latch-up is not predictable, it must be estimated by actual tests. It can be reduced by using epitaxial layer (reduced L.U. sensitivity) or SOI substrate (zero latch-up). They can be destructive if no care is taken at power distribution level. The cancellation of non destructive latch-up requires a reset. Latch-up is expected to disappear with a bias voltage less than 1 volt (in future technologies).

SEB, which occurs in the drain-bulk junction of power MOSFET used in power supply, can kill the whole system.

SEGR sensitivity increases when the gate oxide thickness decreases (advanced technologies), and when the bias voltage increases (power MOSFETs).

SEE sensitivity tests must take into account:

- The energy spectrum of the various particles expected in the actual operation conditions.
- The type and the energy of the particles used for SEE tests (it must represent the worst case among all the particles expected in the actual operation conditions);
- The biasing conditions foreseen in the actual operation conditions;
- The angle between the incident track and the silicon surface (a browsing is required);
- The electrical parameters which could be modified by SEE (a periodical screening of the memories is required, as well as a BER measurement, a bias current monitoring, etc.).

Standard tests have been recently developed to evaluate SEGR.

Reliable guidelines dedicated to other SEE tests are available in specialized literature (however, these guidelines are not yet standard procedures).

VII. Discussion and decisions:

Radiation levels:

- The radiation levels given in the ATLAS Policy on Radiation Tolerant Electronics and in the ATLAS-TC-TDR are not the same.
 - More accurate simulation are requested by Tile Cal Collaboration.
- ⇒ A table containing the most recent data available, including additional calculations requested by Tile Cal, certified by simulation experts, must be published as soon as possible by the RHA-WG.

Test procedures:

- *Standard* irradiation test procedures (TID, NIEL, SEE) would avoid risks and would give normalized results which can be used by all the LHC community. They will also solve the problem of safety factor on dose rate and on neutron fluency rate for CMOS devices.

COTS:

- COTS batches are made of parts which could be issued from numerous manufacturers.
- Margins between targeted radiation levels and failure irradiation levels could be required to take into account the spreading of the COTS radiation tolerance within batches. Statistical analysis could also be useful to estimate the reliability of the radiation hardness of COTS issued from unknown batches.

- Procurement of batches containing COTS issued from known manufacturers could be discussed with vendors in order to avoid unexpected spreading of the radiation tolerance.
- A COTS database containing reliable radiation hardness information would allow a pre-selection of potentially radiation-tolerant COTS and thus would help to save time and money. A list of all the components required by the ATLAS sub-detector groups is required to start this database.

Voltage regulators:

- Positive rad-hard voltage regulators have been developed by SGS-Thomson for the RD 49 collaboration (CERN). Voltages supplied are:
 - . Adjustable regulated voltage from + 1.25 volts to + 8 volts,
 - . Fixed regulated voltage: + 2.5V; + 3.3V, + 4.0V; + 5.0V and + 6.0V.
- Negative rad-hard voltage regulators are currently under development by SGS-Thomson for the RD 49 collaboration. Voltages supplied will be the same (mirrored) than those supplied by the positive voltage regulators.

Improvement and spreading of the knowledge on radiation effects within ATLAS:

- The Radiation Hardness Assurance approach requires a “good knowledge” of the radiation shared within each sub-detector collaboration. A strong background already exists within the RHA-WG and can be improved by discussions with experts, etc. The spreading of this knowledge within ATLAS collaborations can be done by their representatives in the RHA-WG.
- A “Digest of the radiation effects on electronics components and circuits” is currently under preparation within the RHA-WG (M. Dentan). Transparencies based on the first part of this document are already available on the web at the following address:

<http://www.cern.ch/Atlas/GROUPS/FRONTEND/radhard.htm>

Members of the RHA-WG:

- ATLAS collaborations will designate their representative within the RHA-WG.
- The Detector and control system (DCS) collaboration will be invited to participate to subsequent RHA-WG meetings.

Open technical questions:

- How to evaluate low dose rate effects in bipolar devices?
- Is it possible to merge standard NIEL test (neutron) and standard TID tests (γ ^{60}Co) (including post-radiation annealing) into a single test performed with protons?
- What kind of particle and energy shall we use to represent the worst case of ATLAS spectrums in SEE tests?
- Where can we find reliable data on the radiation hardness of passive components (resistor, capacitor, ...)?

- Are there rules to choose between radiation tests on board and radiation tests on elementary devices?
- What are the maximum latch-up, SEU and bit error rates acceptable by each subsystem?
- Can we use a standard FMEA (Failure Mechanisms and Effects Analysis) approach to evaluate the robustness of ATLAS sub-detectors against radiations?
- (...).

Decisions:

WHAT?	WHO?
Designate the representatives of the ATLAS collaborations within the RHA-WG	Each ATLAS collaboration
Publish updated radiation level tables certified by simulation experts	RHA-WG
Establish a list of all the components + total quantities) required by each ATLAS sub-system.	Representatives of each ATLAS collaboration
Propose standard test procedures for cumulated radiation effects.	RHA-WG
Propose standard test procedures for radiation single event effects.	RHA-WG
Define and feed a preliminary COTS database.	COTS-WG
Improve and share knowledge on radiation effects within each ATLAS collaborations.	RHA-WG
Propose a method for statistical analysis.	RHA-WG
Study and propose COTS procurement strategy.	RHA-WG

Appendix 1: Summary of TILE electronics components and test results.

- a. High Voltage bus boards: only connectors => no degradation expected under Tile radiation levels.
- b. Divider boards: only metal film resistors and ceramic capacitors. Tests up to 500 Gy and $2E12$ n.cm² (1 MeV equivalent) => no degradation observed.
- c. Mother boards: Radiation tests not performed.
- d. Adder boards: Radiation tests not performed.
- e. HV micro boards: Targeted irradiation level: 60 Gy and $4.5E11$ n/cm². Problems observed on the micro-controller with can-bus and failure observed on the EEPROM. No problem observed on the flash memory.
- f. HV opto boards: Targeted irradiation level: 60 Gy and $4.5E11$ n/cm². Problems observed on the HV transistor, on the opto-coupler, and on the MUX. No problem observed on the other devices.
- g. 3-in-1 boards: Targeted irradiation level: 500 Gy and $7.5E12$ n/cm². Problems observed on first versions of DAC, amplifiers and analog switches, solved by choosing more radiation-tolerant devices (new type of device).
- h. Integrator boards: Targeted irradiation level: 75 Gy and $1.5E12$ n/cm². ⁶⁰Co irradiation: problem observed on the can-bus; intermittent failure observed on the SRAM, and drift of the conversion factor observed in the DAC-|ACD chain. No problems under neutron irradiation.
- i. Digitized boards: Targeted irradiation level: 500 Gy and $7.5E12$ n/cm². No problem observed on the ADC up to the targeted irradiation level. Most of the other components are still to be tested.

Appendix 2: Summary of LAR electronics components and test results.

Front End Board:

- a. Preamplifiers: Hybrid circuits: no visible dose or neutron effect on noise, gain and speed. GaAs Trinquint chips: good results.
- b. Shapers (BiCMOS 1.2 μm AMS ASIC): no visible dose or neutron effect. Irradiation tests at low dose rate are in progress. SEE tests to be done.
- c. SCA (DMILL ASIC): no visible dose or neutron effect on signal and noise. SEE tests to be done.
- d. SCA controller (XILINK FPGA): failure on dose tests for both 0.35 and 0.25 μm processes. Migration into DMILL ASIC under evaluation (9/99).
- e. Subtractor (Analog Device AD8042): COTS, to be tested.
- f. ADC (Analog Device AD9220 12 bits 5 MHz): failure on dose tests. Could be replaced by AD9042 (successfully tested by CMS). SEE tests to be done.
- g. Optical driver (HP Glink): SEU induces deadtime (see M.L. Andrieux's talk).
- h. Layer sum (Analog Device AD8011): good results. SEE tests to be done.
- i. Timing (TTCrx DMILL chip): chip under development by CERN.
- j. Control Logic: FPGA, to be translated into DMILL.
- k. Voltage regulators: Relies on CERN/STm developments. SEE tests to be done.

Calibration Board:

- a. Fast switch: preliminary tests give satisfactory results; to be continued this fall.
- b. Low offset OPAMPS: no satisfactory results. Custom developments in AMS (7/99) then in DMILL (00).
- c. 16 bits DAC: no satisfactory results. Custom developments in AMS (7/99) then in DMILL (00).
- d. Delays: chip migrated into DMILL.
- e. Control Logic (FPGA Xilinks): to be migrated into DMILL.

Tower builder boards:

- a. OPAMPS: AD8011, AD 8001, HF 1135. Good results. SEE tests to be done.
- b. MUX (DG538): no satisfactory results on COTS. Custom development in DMILL are completed and give satisfactory results.
- c. Delay line passive RCL cots: good results. SEE tests to be done.
- d. Control Logic (FPGA): to be migrated into DMILL.

Power supply:

- Gamma and neutron sensitivity: tests made by BNL on VICOR power supply show failures below the targeted radiation levels. VICOR agreed to replace the sensitive component (optocoupler) by a transformer. Tests made on these modified power supplies show no failure up to the targeted dose and neutron fluence. These power supplies will be followed by rad-hard voltage regulators developed by ST (CERN contract).
- SEE sensitivity: tests must be done in order to check the robustness of the power supplies plus voltage regulators against SEGR (Single Event Gate Rupture) and SEB (Single Event Burn-out) induced by a single ionizing particle (SEGR may destroy the gate of power MOSFETs, SEB may destroy power bipolar transistors).

Appendix 3: Summary of Pixel electronics components and test results.

ASICs

- a. FED (Front-End chip DMILL) for all layers except B layer: Analog cell show no significant resolution or efficiency loss after $7E14 \text{ p.cm}^{-2}$ (tests made on MAREBO chip). SEU rate (1 upset per $3.6E12 \text{ p.cm}^{-2}$) measured with 24 GeV protons complies with Pixels needs. The final FED chip is expected from October 99 DMILL batch.
- b. FEH (Front-End chip Honeywell) for B layer: This chip will be designed and submitted for fabrication (first prototype) in march 99.
- c. Module Controller Chip MCC (DMILL): This chip is expected from October 99 DMILL batch.
- d. DORIC (DMILL): This chip, translated from an AMS radiation-soft version developed by SCT collaboration, is expected from October 99 DMILL batch.

- e. VDC (VCSEL Driver Chip, DMILL): This chip, translated from an AMS radiation-soft version developed by SCT collaboration, is expected from October 99 DMILL batch.
- f. LVDS (Low Voltage Differential Signal, DMILL): This chip is expected from October 99 DMILL batch. It will not enter into in the module; but will be used only for test purposes (a radiation hard chip is required for on-line tests).

COTS:

- a. VCSEL: Pixel collaboration relies on COTS selection made by SCT collaboration.
- b. PIN diode: Pixel collaboration relies on COTS selection made by SCT collaboration.
- c. Fujikura SIMM 50/60/125/250 optical fibers: tested up to 30 Mrads.

Sensor:

- Rad-hard design developed by ATLAS Pixel collaboration. Proton tests made at LBL and at CERN. According to the tests results, acceptable performances are expected after the irradiation doses and fluences foreseen in ATLAS, provided sensors are properly handled to avoid long term reverse annealing.

Appendix 4: BER prediction using the first model:

- $\sigma_{n,p}$ = cross section of n,p reaction.
- $\sigma_{n,\alpha}$ = cross section of n, α reaction.
- σ_p = \int mean cross section of *upsets* induced by n,p reaction.
=> $\sigma_p = \int_{E_n} [\sigma_{n,p}(E_n) * \Phi_n(E_n) dE_n] / \int_{E_n} \Phi_n(E_n) dE_n$.
- σ_α = mean cross section of *upsets* induced by n, α reaction.
=> $\sigma_\alpha = \int_{E_n} [\sigma_{n,\alpha}(E_n) * \Phi_n(E_n) dE_n] / \int_{E_n} \Phi_n(E_n) dE_n$.
- $\langle \sigma_{tot} \rangle = \sigma_p + \sigma_\alpha$ ($\langle \sigma_{tot} \rangle$ depends on the incident neutron spectrum).
- $\langle \sigma_{tot} \rangle_{(EXP)}$ = $\langle \sigma_{tot} \rangle$ calculated with the experimental neutron spectrum (ex: CERI)
- $\langle \sigma_{tot} \rangle_{(ATLAS)}$ = $\langle \sigma_{tot} \rangle$ calculated with the simulated ATLAS neutron spectrum;
- $\Phi_n_{(ATLAS)}$ = ATLAS neutron flux;
- $\Phi_n_{(CERI)}$ = CERI neutron flux;
- N = total number of Glink in ATLAS;
- $BER_{(EXP)}$ = Bit Error Rate *measured* using the experimental spectrum (ex: CERI);
- $BER_{(ATLAS)}$ = Bit Error Rate *estimated* for ATLAS LAR optical links.

$$\Rightarrow BER_{(ATLAS)} = BER_{(CERI)} * \{ \langle \sigma_{tot} \rangle_{(ATLAS)} / \langle \sigma_{tot} \rangle_{(EXP)} \} * \{ \Phi_n_{(ATLAS)} / \Phi_n_{(CERI)} \} * N.$$